REMARKS

Status of Claims

Claims 1-35 are pending in the application. Claims 1-7, 9-26 and 28-35 have been rejected. Claims 8 and 27 are objected to. Claims 2-4, 20, 21, and 23 have been amended per the Examiner's suggestions.

Specification

The specification has been objected to as failing to provide proper antecedent basis for the claimed subject matter. The Examiner states: "Correction of the following is required:"

> "Claims 2 and 20 state that the cache coherency protocol of claims 1 and 18 interfaces with the storage controller. However, the cache coherency protocol is self-contained within the bounds of the instruction and data caches of the central processing unit and is merely a statement of policy. It is unclear from the specification how this protocol interfaces with the storage controller because interfacing implies communication between independent entities, whereas the policy statements comprising the protocol do not provide a means for such communication."
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> "Claims 3, 4, 21 and 23 state that the cache coherency protocol of claims 1 and 18 interfaces with existing cache handling requirements. Again, it is unclear from the specification how the policy statements comprising the protocol of claims 1 and 18 interface with the cache handling requirements, which likewise are merely statements of necessary conditions and do not provide a means for the communication implied by interfacing."
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> "For the purposes of examination, claims 2 and 20 will be interpreted to teach that the cache coherency protocol of claims 1 and 18 operates in cooperation with the processor system cache coherency protocol employed by the storage controller."
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> "Claims 3, 4, 21 and 23 will be interpreted to teach that the cache coherency protocol of claims 1 and 18 operates in cooperation with existing cache handling requirements."
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> "It is suggested that claims 2-4, 20, 21 and 23 be amended to reflect the above interpretations."

Applicants appreciate the Examiner's observations and have amended Claims 2 – 4, 20, 21, and 23 as suggested to address the Examiner's concerns.

Claim Rejections - 35 USC § 103

Claims 1-4 and 13-17 have been rejected under 35 U.S.C. 103(a) as being unpatentable over suggested admitted prior art (denoted by the Examiner as APA) in view of Gaskins U.S. Patent No. 5,930,821, hereinafter referred to as Gaskins, in further view of Anderson U.S. Patent No. 3,735,360, hereinafter Anderson. Applicants respectfully traverse. The Examiner states in the Office Action:

> "As in claims 1-4, and 16-17 APA discloses a conventional multi-processor computer system comprising a plurality of central processing units each including an execution unit, an instruction unit, and a plurality of caches including separate instruction and operand caches, where the central processing units are connected to a shared main memory through a storage controller (Page 1, lines 5-22). It is noted that an existing system cache coherency protocol and cache handling requirements employed by the storage controller are inherent in the system of APA in order to maintain consistency of the shared data between the caches in the processors."
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> "APA does not teach subjecting the instruction and operand caches to a cache coherency protocol with interlocks on cache block access, nor does APA teach the particular cache coherency protocol as required by claim 1."
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> "APA also does not teach that the instruction and operand cache coherency protocol operates in cooperation with the existing cache coherency protocol and cache handling requirements as required by claims 2-4."
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> "APA also does not teach shared read status, exclusive status and read-only status as required by claims 13-15."
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> "Gaskins teaches a system comprising separate code (i.e. instruction) and data (i.e. operand) caches supporting self-modifying code by subjecting the code and data caches to a cache coherency protocol with interlocks on cache block access (Fig. 6, elements 605 and 607; column 6, line 64 to column 7, line 15; column 9, lines 19-24)."
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> "Anderson teaches a system comprising a pair of parallel and independent caches subjected to a cache coherency protocol (Fig. 1, elements 10, 15 and 16; column 5, lines 18-26), where a cache can have the only copy of a block of data (i.e. exclusive) or one of multiple copies of a block of data (i.e. shared), indicated by a fetch-only bit (Fig. 3, element 62; column 8, lines 10-21) in the cache directory (Fig. 3, element 27; column 5, lines 46-49)."
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> "Anderson further describes that when the block of data has exclusive status in a cache, the block may be stored into (i.e. written), but when the block of data is shared it may only be read (Column 8, lines 22-35). This latter state corresponds to a read-only status. Anderson further emphasizes that before a block of data can be stored into, other existing copies must be invalidated and exclusive ownership must be obtained (Column 8, lines 35-39)."
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> "Therefore, the protocol described by Anderson may be summarized

as:

allowing shared read access by a first cache and second cache to a cache block if the cache block has read-only status in the first cache and the second cache;

allowing read and write access by the first cache and preventing access by the second cache to the cache block if the cache block has exclusive status in the first cache; and

interlocking write access to the cache block by the first cache with exclusive status if the cache block has read-only status in the second cache;"

"Regarding claim 1, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to subject the instruction and operand caches to a cache coherency protocol with interlocks on cache block access as taught by Gaskins, in the system of APA, in order to support self-modifying code as taught by Gaskins."

"Further regarding claim 1, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use the cache coherency protocol taught by Anderson, in the system made obvious by the combination of APA and Gaskins, due to the similarity in nature of the problems, namely to provide coherency between a pair of parallel caches sharing a common main storage where the same information may be stored in either cache."

"Regarding claims 2-4, although the combination of APA, Gaskins and Anderson does not explicitly teach the instruction and operand cache coherency protocol operate in cooperation with the existing cache coherency protocol and cache handling requirements, Examiner takes Official Notice that it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to do so. As noted above, APA teaches a system with an existing cache coherency protocol and cache handling requirements that allow a plurality of central processing units to share access to a main memory. As also noted above, the combination of APA, Gaskins and Anderson teaches a cache coherency protocol for maintaining consistency between an instruction and operand cache within the central processing units of APA. One skilled in the art would recognize that the first protocol does not preclude the second, and that both would be necessary for the system to properly function."

"Claims 13-15 are rejected using the same rationale as for the rejection of claim 1, noting the teachings regarding shared, exclusive and read-only status contemplated by Anderson."

Applicants respectfully contend that explanation in the Office Action mischaracterizes the teachings of suggested admitted prior art, Gaskins, and/or Anderson and that the cited references do not teach or disclose each element of the invention. For an obviousness rejection to be proper, the Examiner must meet the burden of establishing a *prima facie* case of obviousness. *In re Fine*, U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988). The Examiner must

meet the burden of establishing that all elements of the invention are disclosed in the prior art; that the prior art relied upon, coupled with knowledge generally available in the art at the time of the invention, must contain some suggestion or incentive that would have motivated the skilled artisan to modify a reference or combined references; and that the proposed modification of the prior art must have had a reasonable expectation of success, determined from the vantage point of the skilled artisan at the time the invention was made. *In re Fine*, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988); *In re Wilson*, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970); *Amgen v. Chugai Pharmaceuticals Co.*, 927 U.S.P.Q.2d, 1016, 1023 (Fed. Cir. 1996).

With regard to Claims 1-4 and 13-17, Applicants respectfully contend that neither the suggested admitted prior art, Gaskins, nor Anderson teach or disclose each element of the invention. Specifically, as stated above for Claim 1, neither the suggested admitted prior art, Gaskins, nor Anderson teach or disclose, "allowing shared read access by said instruction cache and said operand cache to a cache block if said cache block has read only status in said instruction cache and said operand cache; allowing read and write access by said operand cache and preventing access by said instruction cache to said cache block if said cache block has exclusive status in said operand cache; and interlocking access to said cache block by said operand cache with exclusive status in said operand cache if said cache block has read-only status in said instruction cache." In particular, Applicants respectfully contend that the Examiner has mischaracterized the teachings of Anderson while applying that reference to the claimed invention. The Examiner relies, on the Anderson at Col. 8 lines 22-39. However, it is evident from the disclosure of Anderson that the cache coherency protocol disclosed therein only addresses sharing data between two processors, there is no teaching with regard to addressing cache coherency for instructions that later modify themselves. Moreover, Gaskins includes no teaching with respect to cache coherency with storage controller and multiple processors. Therefore, because neither the admitted prior art, Gaskins, nor Anderson disclose or teach an element of the invention they cannot render Applicant's claims unpatentable. Thus, Claims 1-4 and 13-17 are allowable, the rejections are improper, and they should be withdrawn.

In addition, Claims 2-17 include the same limitations as Claim 1 an allowable claims, and therefore, are also allowable, and improperly rejected. Thus, the rejections of Claims 2-17 should be withdrawn. Moreover, Claims 2-17 are dependent from Claim 1, an allowable claim by reason of the arguments presented above, and therefore Claims 2-17 must also be

allowable. Thus, Claims 2-17 are allowable, the rejections are improper, and they should be withdrawn.

Furthermore, with regard to Claims 1-4 and 13-17 and more specifically Claim 1, Applicants respectfully maintain that the Examiner has used an improper standard in arriving at the rejection of the above claims under §103, based on improper hindsight which fails to consider the totality of Applicants' invention and to the totality of the cited references. More specifically the Examiner has used Applicant's disclosure to select portions of the cited references to allegedly arrive at Applicants' invention. In doing so, the Examiner has failed to consider the teachings of the references or Applicants' invention as a whole in contravention of §103.

In particular, the Examiner has provided no explanation or suggestion for the motivation to make the suggested combination, nor has the Examiner identified where in the cited references or the art teaching of such motivation may be found. *In re Fine* specifically requires that the Examiner must meet the burden of establishing the suggestion or incentive that would have motivated the skilled artisan to modify a reference or combined references. The explanation in the Office Action provides no such indication as to where in the references or the art such a suggestion may be found. There is no specific teaching in the prior art, or Gaskins that would motivate one skilled in the art to look to Anderson, or vice versa as suggested by the Examiner. In fact, Applicants respectfully suggest that it should be appreciated that if such motivation did exist, Gaskins surely would have disclosed and employed such a configuration for his system. Gaskins was clearly aware of cache memory systems and multiple processors. See background and reference to text. Gaskins was specifically aware that other devices could readily be attached to the bus, See col. 2 lines 13-14. However, Gaskins clearly did not envision expanding the cache coherency protocol for split code and data cache to address a storage controller and additional microprocessors as claimed by the Applicants. Therefore, there is no suggestion or motivation to combine the cited references. Clearly, the Examiner has employed improper hindsight to merely locate references to find the claimed elements without providing suggestion for their combination. Therefore, the Examiner has not made a prima facie case for obviousness and Claims 1-4 and 13-17 may not be rendered unpatentable as suggested. Therefore, Claims 1-4 and 13-17 are allowable, the rejections are improper, and they should be withdrawn.

Claims 5-7, 9 and 11-12 have been rejected under 35 U.S.C. 103(a) as being unpatentable over suggested admitted prior art (denoted by the Examiner as APA) in view of Gaskins U.S. Patent No. 5,930,821, hereinafter referred to as Gaskins, in further view of Anderson U.S. Patent No. 3,735,360, hereinafter Anderson. As applied to claim 3 above, and further in view of Mahalingaiah U.S. Patent No. 6,073,217, hereinafter Mahalingaiah. Applicants respectfully traverse. The Examiner states in the Office Action:

> "APA, Gaskins and Anderson are relied upon for the teachings relative to claim 3 as above."
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> "As in claim 5, Gaskins further teaches that when an instruction fetch is requested, providing the instruction cache read-only status for a requested cache block (Fig. 2, element 205; column 2, lines 18-20; Fig. 8; column 8, lines 58-61), where it is readily apparent from Gaskins that the status for a block in the instruction cache must be read-only because the control unit (i.e. instruction unit) (Fig. 2, element 222) may only fetch instructions and maintains them prior to execution (Column 2, lines 18-27)."
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> "Also as in claim 5, Anderson further teaches that when data is required to be stored or updated, an associated cache block's status is evaluated for a desired storage address in a first cache (Fig. 2; column 8, line 55 to column 9, line 3) and a request for exclusive status is transmitted to a storage control unit and a cross-interrogate signal is transmitted to a second cache (Fig. 2; column 9, lines 4-19)."
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> "The rationale derived from Anderson in the rejection of claim 3 above is incorporated herein for the teaching of storing in the first cache after exclusive status is obtained via the storage control unit following a response from the cross interrogation."
>
> "As in the rejection of claim 3 above, it is noted that the protocol applied to the first and second caches in Anderson is applied to the operand and instruction cache."
>
> "The combination of APA, Gaskins and Anderson does not teach the following steps as required by claim 5-6 and 9, however, these steps are taught by Mahalingaiah:"
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> "buffering cache block addresses in a register-file (Fig. 2, element 48) in an instruction cache (Figs. 1 and 2, element 22) corresponding to fetched unexecuted instructions in an instruction buffer in the instruction unit (Column 3, lines 1-7; column 8, lines 34-37);"
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> "discarding and refetching data in the instruction cache if the associated cache block in the instruction cache matches the desired storage address (Column 3, lines 8-12; column 8, lines 41-59);"
>
> "discarding and refetching data in the instruction buffer and re-buffering cache locations in the register if an instruction stream of an execution unit (Fig. 1, element 28) changes (i.e. if the code is self-modified, see Instant Application, page 6, lines 22-24) (Column 5, lines 13-29 and 54-58; column 8, lines 4 1-59; column 9, lines 48-60); and"

discarding data in the instruction buffer and discarding the cache locations in the register if the execution unit completes execution of fetched instructions (Column 4, lines 13-15; column 8, lines 41-59)."

"Mahalingaiah teaches that the above steps allow correct execution of self-modifying code (Column 3, lines 12-14; column *5, lines 54-58).*"

"Regarding claims 5-6 and 9, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use the teachings of Mahalingaiah enumerated above, in the system made obvious by the combination of APA, Gaskins and Anderson, in order to allow correct execution of self-modifying code as taught by Mahalingaiah."

"As in claim 7, Anderson further teaches that when exclusive ownership of a cache block is requested, all other copies whether exclusive or read-only are invalidated (Column 8, lines 35-39; column 9, lines 20-32)."

"As in claims 11, Anderson teaches that the cross-interrogation of the cache block address is accomplished via a directory lookup in the storage control unit (Fig. 1, elements 27-28; column 4, lines 20-27 and 56-62; column 5, lines 45-48)."

"Regarding claim 12, although the combination of APA, Gaskins, Anderson and Mahalingaiah does not teach that the cache directory and register-file comprise six locations, such limitations are merely a matter of design choice and would have been obvious in the system of APA, Gaskins, Anderson and Mahalingaiah. The combination of APA, Gaskins, Anderson and Mahalingaiah teaches both a directory and register file. The limitations in claim 12 of the instant application do not define a patentably distinct invention since both are directed toward providing storage for indexing cache contents and instruction fetch unit contents. The number of locations is inconsequential for the invention as a whole and presents no new or unexpected result. Therefore, to use six locations would have been an obvious design choice to one of ordinary skill in the art at the time of invention by applicant."

With regard to Claims 5-7, 9, 11-12, 28, and 29-30, Applicants respectfully contend that neither admitted prior art, Gaskins, Anderson, nor Mahalingaiah, teach or disclose each element of the invention as stated above for Claim 1. Therefore, because neither the admitted prior art, Gaskins, Anderson, nor Mahalingaiah, disclose or teach an element of the invention they cannot render Applicant's claims unpatentable. Thus, Claims 5-7, 9 and 11-12 are allowable, the rejections are improper, and they should be withdrawn.

Furthermore, with regard to Claims 5-7, 9 and 11-12 and more specifically Claim 1 and 5, Applicants respectfully maintain once again that the Examiner has used an improper standard in arriving at the rejection of the above claims under §103, based on improper hindsight which fails to consider the totality of Applicants' invention and to the totality of the cited references. More specifically the Examiner has used Applicant's disclosure to select portions of the cited references to allegedly arrive at Applicant's invention. In doing so, the

Examiner has failed to consider the teachings of the references or Applicant's invention as a whole in contravention of §103.

In particular, the Examiner has provided no explanation or suggestion for the motivation to make the suggested combination, nor has the Examiner identified where in the cited references or the art teaching of such motivation may be found. *In re Fine* specifically requires that the Examiner must meet the burden of establishing the suggestion or incentive that would have motivated the skilled artisan to modify a reference or combined references. The explanation in the Office Action provides no such indication as to where in the references or the art such a suggestion may be found. As stated for Claim 1 above, there is no specific teaching in the prior art, or Gaskins that would motivate one skilled in the art to look to Anderson, or vice versa as suggested by the Examiner. Similarly, Applicants respectfully suggest that there is no specific teaching in the prior art, Gaskins, or Anderson, that would motivate one skilled in the art to look to Mahalingaiah, or vice versa as suggested by the Examiner. In fact, Applicants respectfully suggest once again, that it should be appreciated that if such motivation did exist, Gaskins and/or Mahalingaiah surely would have disclosed and employed such a configuration for his system. Gaskins and/or Mahalingaiah were clearly aware of cache memory systems and multiple processors. See Mahalingaiah Fig. 4. However, neither Gaskins nor Mahalingaiah envisioned expanding the cache coherency protocol for split code and data cache to address a storage controller and additional microprocessors. Therefore, there is no suggestion or motivation to combine the cited references. Clearly, the Examiner has employed improper hindsight to merely locate references to find the claimed elements without providing suggestion for their combination. Therefore, the Examiner has not made a prima facie case for obviousness and Claims 5-7, 9 and 11-12 may not be rendered unpatentable as suggested. Therefore, Claims 5-7, 9 and 11-12 are allowable, the rejections are improper, and they should be withdrawn.

Claim 10 has been rejected under 35 U.S.C. 103(a) as being unpatentable over the Examiner's suggested APA in view of Gaskins and Anderson, and further in view of Mahalingaiah as applied to claim 5 above, and further in view of Handy (The Cache Memory Book, Jim Handy, 1998). Applicants respectfully traverse. The Examiner states in the Office Action:

> "APA, Gaskins, Anderson and Mahalingaiah are relied upon for the teachings relative to claim 5 as above."

"Anderson further teaches an existing cache handling requirement whereby entries in the cache are replaced according to a replacement algorithm (Column 9, lines 33-39)."

"The combination of APA, Gaskins, Anderson and Mahalingaiah does not teach that the replacement algorithm is a least-recently used replacement algorithm as required by claim 10."

"Handy teaches a least recently used cache block replacement algorithm used to determine where to place new blocks of data in a cache (Page 57, paragraph 2)."

"It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use the least recently used replacement algorithm taught by Handy, in the system made obvious by the combination of APA, Gaskins Anderson and Mahalingaiah, for the purpose of determining where to place new blocks of data in the cache as taught by Handy."

With regard to Claim 10, Applicants respectfully maintain that the Examiner has used an improper standard in arriving at the rejection of the above claims under §103, based on improper hindsight, which fails to consider the totality of Applicants' invention and to the totality of the cited references. In particular, the Examiner has provided no explanation or suggestion for the motivation to make the suggested combination, nor has the Examiner identified where in the cited references or the art teaching of such motivation may be found. As stated for Claim 1 above, there is no specific teaching in the prior art, or Gaskins that would motivate one skilled in the art to look to Anderson, or vice versa as suggested by the Examiner. Similarly, as stated for Claim 5, Applicants respectfully suggest that there is no specific teaching in the prior art, Gaskins or Anderson that would motivate one skilled in the art to look to Mahalingaiah, or vice versa as suggested by the Examiner. Similarly, there is no teaching or motivation to now look also to Handy. In fact, because neither Gaskins nor Mahalingaiah did teach the claimed invention despite being aware of those elements of the cited references clearly teaches away from the suggested combination and indicates that the invention is not obvious as the motivation to combine the teachings of the suggested prior art, and/or Anderson and Gaskins or Mahalingaiah clearly is not present. Therefore, there is no suggestion or motivation to combine the cited references. Clearly, the Examiner has improper hindsight to merely locate references to find the claimed elements without providing suggestion, teaching or motivation for their combination. Therefore, the Examiner has not made a prima facie case for obviousness and Claim 10 may not be rendered unpatentable as suggested. Therefore, Claim 10 is allowable, the rejection is improper, and it should be withdrawn.

Regarding Claims 18-35, Applicants arguments for Claims 1, 5 and the like are equally applicable. Therefore, they have not been repeated and addressed in detail. For example, like Claim 1, with regard to Claim 18, Applicants respectfully maintain that the Examiner has used an improper standard in arriving at the rejection of the above claims under §103, based on improper hindsight. In particular, the Examiner has provided no explanation or suggestion for the motivation to make the suggested combination, nor has the Examiner identified where in the cited references or the art teaching of such motivation may be found. As stated for Claim 1 above, there is no specific teaching in the prior art, or Gaskins that would motivate one skilled in the art to look to the prior art, or vice versa as suggested by the Examiner. Similarly, as stated for Claim 5, Applicants respectfully suggest that there is no specific teaching in the prior art, Gaskins or the prior art that would motivate one skilled in the art to look to Mahalingaiah, or vice versa as suggested by the Examiner. Once again, because neither Gaskins nor Mahalingaiah did teach the claimed invention despite being aware of those elements of the cited references clearly teaches away from the suggested combination and indicates that the invention is not obvious as the motivation to combine the teachings of the suggested prior art, and/or Anderson and Gaskins or Mahalingaiah clearly is not present. Therefore, there is no suggestion or motivation to combine the cited references. Clearly, the Examiner has improper hindsight to merely locate references to find the claimed elements without providing suggestion, teaching or motivation for their combination. Therefore, the Examiner has not made a prima facie case for obviousness and Claim 18 may not be rendered unpatentable as suggested. Therefore, Claim 18 is allowable, the rejection is improper, and it should be withdrawn. Similarly, Claims 19-35 include the same limitations as Claim 18, an allowable claim, and therefore, are also allowable and improperly rejected. Thus, the rejections of Claims 19-35 should be withdrawn. Moreover, Claims 19-35 are dependent from Claim 18, an allowable claim by reason of the arguments presented above, and therefore Claims 19-35 must also be allowable. Thus, Claims 19-35 are allowable, the rejections are improper, and they should be withdrawn.

The arguments and amendments presented herein are made for the purposes of better defining the invention, rather than to overcome the rejections for patentability. The claims have not been amended to overcome the prior art and therefore, no presumption should attach that either the claims have been narrowed over those earlier presented, or that subject matter or equivalents thereof to which the Applicants are entitled has been surrendered. Allowance of the claims is respectfully requested in view of the above remarks. Moreover, no amendments as presented alter the scope of the claimed invention and therefore cannot necessitate a new grounds rejection.

It is believed that the foregoing remarks are fully responsive to the Office Action and that the claims herein should be allowable to the Applicants. In the event the Examiner has any queries regarding the instantly submitted response, the undersigned respectfully requests the courtesy of a telephone conference to discuss any matters in need of attention.

If there are additional charges with respect to this matter or otherwise, please charge them to Deposit Account No. 09-0463.

Respectfully Submitted,

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Date: July 8, 2004